ABSTRACT OF THE DISCLOSURE

Methods and apparatuses for designing a plurality of integrated circuits (ICs) from a language representation of hardware. In one example of a method, a technology independent RTL (register transfer level) netlist is partitioned between representations of a plurality of ICs. In a typical example of the method, a hardware description language (HDL) code is written and compiled without regard to splitting the design among multiple ICs. After compilation, a partition of the technology independent RTL netlist, obtained from the compilation, is performed among the multiple ICs. After a partition, the technology independent RTL netlist is mapped to a particular target technology (e.g. a particular IC vendor's architecture for implementing logic circuitry), and place and route tools may be used to create the design in multiple ICs (e.g. field programmable gate arrays). In an example of another method, an HDL code is compiled to produce an RTL netlist representation which specifies a plurality of ICs in which logic, designed for placement on one of the plurality of ICs, is replicated for placement on another one of the plurality of ICs. In a typical example of this method, the HDL code is written and compiled without regard to splitting the design among multiple ICs and a partition operation is performed on the RTL netlist from the results of the compiled HDL code. The partition operation produces multiple ICs and selected logic may then be replicated on the multiple ICs. In an example of another method, an HDL code is compiled to produce an RTL netlist representation which includes at least one RTL component. The one RTL component is split into multiple RTL components, each of which is designed for placement on a separate IC.